Amendments to the Claims:

This following listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (previously presented): A device for computing circuit paths between a first node and a second node within a network, the network including a plurality of elements, the device comprising:

a memory;

a route generator, the route generator being arranged to generate a primary circuit path between the first node and the second node, the primary circuit path including a first element selected from the plurality of elements, wherein the route generator is ~~**configured**~~ configurable to selectively generate a nodal diverse alternate circuit path when a nodal diverse constraint is input~~**, and further configured to generate**~~ and a link diverse alternate circuit path when a link diverse constraint is input, the input further being arranged to specify circuit characteristics for the primary circuit path and for the alternate circuit path; and

a list mechanism, the list mechanism being stored in the memory, the list mechanism being arranged to identify the first element, wherein the route generator is further arranged to generate an alternate circuit path between the first node and the second node using the list mechanism and the input, wherein the alternate circuit path does not include the first element identified by the list mechanism.

Claims 2-3 (canceled)

Claim 4 (original): A device as recited in claim 1 wherein the plurality of elements includes a protected link, the list mechanism further being arranged to identify the protected link, wherein the alternate circuit path does not include the protected link.

Claim 5 (currently amended): A device as recited in claim 1 wherein the route generator is arranged to generate the primary circuit path that includes the first element and a set of elements selected from the plurality of elements, and the list mechanism is arranged to identify

the first element and the set of elements as being inaccessible for use in subsequently generating the alternate circuit path.

Claim 6 (original): A device as recited in claim 5 wherein the plurality of elements includes a protected link, the list mechanism further being arranged to identify the protected link as being inaccessible for use in generating the alternate circuit path.

Claim 7 (canceled)

Claim 8 (previously presented): A device as recited in claim 1 wherein when the nodal diverse constraint is input, the first element is a node.

Claim 9 (previously presented: A device as recited in claim 1 wherein when the link diverse constraint is input, the first element is a link.

Claim 10 (original): A device as recited in claim 1 wherein the device is associated with the first node.

Claim 11 (original): A device as recited in claim 1 wherein the route generator is further arranged to implement the primary circuit path and the alternate circuit path.

Claims 12-18 (canceled)

Claim 19 (currently amended): An element for use in an optical network, the optical network including a plurality of nodes, the plurality of nodes including a destination node, the optical network further including a plurality of links, the element comprising:

a memory;

a route generator, the route generator being arranged to compute a first circuit path between the element and the destination node, the first circuit path including a first link included in the plurality of links, wherein the route generator is ~~**configured**~~ configurable to selectively generate a nodal diverse alternate circuit path when a nodal diverse constraint ~~**in put**~~ is input~~**, and further configured to generate**~~ and a link diverse alternate circuit path when a link diverse constraint is input, the input further being arranged to specify circuit characteristics for the first circuit path and for the second circuit path; and

a list, the list being stored in the memory, the list including a plurality of identifiers, the plurality of identifiers being arranged to identify selected links included in the plurality of links, the plurality of identifiers including a first identifier that identifies the first link, wherein the route generator is further arranged to compute the second circuit path using the list and the input, wherein the second circuit path includes a second link included in the plurality of links and does not include the selected links identified by the plurality of identifiers included in the list, wherein a failure of any of the selected links identified by the plurality of identifiers included in the list does not affect computing of the second circuit path.

Claim 20 (original): An element according to claim 19 wherein the selected links included in the plurality of links include a protected link.

Claim 21 (original): An element according to claim 19 wherein the element is a source node.

Claim 22 (original): An element according to claim 19 wherein the route generator is further arranged to identify the first link, to create the first identifier that identifies the first link, and to place the first identifier that identifies the first link in the list.

Claim 23 (original): An element according to claim 22 wherein the route generator is still further arranged to generate the plurality of identifiers that are arranged to identify the selected links included in the plurality of links and to place the plurality of identifiers that are arranged to identify the selected links included in the plurality of links in the list.

Claim 24 (currently amended): An element for use in an optical network, the optical network including a plurality of nodes, the plurality of nodes including a destination node, the optical network further including a plurality of links, the element comprising:

a memory;

a route generator, the route generator being arranged to compute a first circuit path between the element and the destination node, the first circuit path including a first node included in the plurality of nodes, wherein the route generator is configurable to selectively generate a nodal diverse alternate circuit path when a nodal diverse constraint ~~**in put**~~ is input~~**, and further configured to generate**~~ and a link diverse alternate circuit path when a link diverse

constraint is input, the input further being arranged to specify circuit characteristics for the first circuit path and for the second circuit path; and

a list, the list being stored in the memory, the list including a first identifier, the first identifier being arranged to identify the first node, wherein the route generator is still further arranged to compute a second circuit path using the list and the input, wherein the second circuit path includes a second node included in the plurality of links and does not include the first node and a failure of the first node does not affect computing the second circuit path.

Claim 25 (original): An element according to claim 24 wherein the list further includes a second identifier, the second identifier being arranged to identify a protected link included in the plurality of links, wherein the second circuit path does not include the protected link.

Claim 26 (currently amended): An element according to claim ~~23~~ 24 wherein the element is a source node.

Claim 27 (currently amended): An element according to claim ~~23~~ 24 wherein the route generator is further arranged to identify the first node, to create the first identifier that identifies the first node, and to place the first identifier that identifies the first node in the list.

Claims 28-36 (canceled)

Claim 37 (previously presented): The device of claim 1 wherein the route generator is arranged to generate the primary circuit path and the alternate circuit path as nodal diverse paths in which the primary circuit path and the alternate circuit path have no common nodes between the first node and the second node, and wherein when the primary circuit path and the alternate circuit path are the nodal diverse paths, the first element is a node.

Claim 38 (previously presented): The device of claim 1 wherein the route generator is arranged to generate the primary circuit path and the alternate circuit path as link diverse circuit paths in which the primary circuit path and the alternate circuit path share no links between the first node and the second node, and wherein when the primary circuit path and the alternate circuit path are the link diverse circuit paths, the first element is a link.

Claim 39 (currently amended): A device for computing circuit paths between a first node and a second node within a network, the network including a first plurality of elements and at least one protected element, the device comprising:

a memory;

a route generator, the route generator being arranged to generate a primary circuit path between the first node and the second node, the primary circuit path including the first plurality of elements, wherein the route generator is configurable to selectively generate a nodal diverse alternate circuit path when a nodal diverse constraint is input~~, and further configured to generate~~ and a link diverse alternate circuit path when a link diverse constraint is input, the input further being arranged to specify a load characteristic that is to be accounted for when the alternate circuit path is generated; and

a list mechanism, the list mechanism being stored in the memory, the list mechanism being arranged to identify the first plurality of elements and the at least one protected element, wherein the route generator is further arranged to generate an alternate circuit path between the first node and the second node using the list mechanism and the input, wherein the alternate circuit path does not include the first plurality of elements and the at least one protected element identified by the list mechanism.

Claim 40 (previously presented): A device as recited in claim 39 wherein the first plurality of elements are links if the input specifies a link diverse constraint.

Claim 41 (previously presented): A device as recited in claim 39 wherein the first plurality of elements are nodes if the input specifies a nodal diverse constraint.

Claim 42 (previously presented): A device as recited in claim 39 wherein the list mechanism is a tabular list.

Claim 43 (previously presented): A device as recited in claim 42 wherein the tabular list includes a heading area that identifies the first plurality of elements and a heading area that identifies the at least one protected element.

Claim 44 (previously presented): A method for computing circuit paths between a first node and a second node within a network, the network including a plurality of elements, the network comprising:

receiving an input, the input specifying a nodal diverse constraint or a link diverse constraint for an alternate circuit path between the first node and the second node relative to a primary circuit path between the first node and the second node, the input further being arranged to specify circuit characteristics for the primary circuit path and for the alternate circuit path;

generating the primary circuit path, the primary circuit path including a first element selected from the plurality of elements, wherein generating the primary circuit path includes accounting for the specified circuit characteristics;

creating a list, the list being arranged to identify the first element;

storing the list in a memory; and

generating a nodal diverse alternate circuit path when a nodal diverse constraint is received and generating a link diverse alternate circuit path when a link diverse constraint input is received, the alternate circuit path to not include the first element and to account for the specified circuit characteristics, wherein generating the alternate circuit path includes accessing the stored list and identifying the first element stored in the first list as being blocked from use in routing the alternate circuit path.

Claim 45 (previously presented): A method as recited in claim 44 wherein the specified circuit characteristics include one selected from a group including a shortest path characteristic and a load balancing characteristic.

Claim 46 (previously presented): A device as recited in claim 1 wherein the nodal diverse constraint specifies that any nodes in the primary circuit path between the first node and the second node are not included in the alternate circuit path and wherein the link diverse constraint specifies that any links in the primary circuit path between the first node and the second node are not included in the alternate circuit path.

Claim 47 (previously present): The device of claim 1 wherein the circuit characteristics include a load characteristic.